REPLY UNDER 37 CFR 1.116
-EXPEDITED PROCEDURE-
EXAMINING GROUP 2817

REMARKS

Claims 1-8 are pending in the application and are presented for reconsideration. The remaining independent claims are 1, 6, and 7.

By the foregoing amendments, claims 1 and 7 are sought to be amended.

These changes are believed not to introduce new matter, and their entry is respectfully requested. The claims have been amended merely to clarify the claims and expedite the prosecution of the application, not to overcome any cited references.

Based on the above Amendment and the following Remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections, and withdraw them.

The acceptance of the drawings is noted.

Claim 7 has been objected to because of an informality. The Examiner has requested correction of "second resistor" to –third resistor–. Claim 7 has been amended in view of the Examiner's comments and suggestions. Withdrawal of the objection is respectfully requested.

Rejections under 35 U.S.C. §103

The Examiner has rejected claims 1-2 and 6 under the obviousness provisions of 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Published Patent Application No. 2002/0063601 ("Yamamoto") in view of U.S. Patent No. 6,549,076 ("Kuriyama").

Claim 1 has been amended merely to correct a typographical error

REPLY UNDER 37 CFR 1.116
-EXPEDITED PROCEDURE-
EXAMINING GROUP 2817

Based on the above Amendment and the following Remarks, Applicant respectfully requests that the Examiner reconsider the rejection, and withdraw it.

Applicant respectfully submits that there is no motivation or suggestion to combine Yamamoto and Kuriyama. "35 U.S.C. § 103 authorizes a rejection where, to meet the claim, it is necessary to modify a single reference or to combine it with one or more others. After indicating that the rejection is under 35 U.S.C. § 103, there should be set forth [by the Examiner] (1) the difference or differences in the claim over the applied references, (2) the proposed modification of the applied references necessary to arrive at the claimed subject matter, and (3) an explanation of why such proposed modification would be obvious." MPEP § 706.02; emphasis added.

Applicant respectfully asserts that the combination suggested by the Examiner's rejection under 35 U.S.C. § 103 is improper. It is well settled law that when making a rejection under 35 U.S.C. § 103, the Examiner has the burden of establishing a prima facie case of obviousness. The Examiner can satisfy this burden "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references" in the manner suggested by the Examiner. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). "[E]lements of separate prior patents [and/or publications] cannot be combined when there is no suggestion of such combination anywhere in those patents [and/or publications]...; and a court should avoid hindsight..." (emphasis added; annotations within square brackets). Panduit Corp. v. Dennison Mfg. Co., 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), citing ACS Hospital Systems, Inc. v. Montefiore Hospital, 220 USPQ 929, 933 (Fed. Cir. 1984), and W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983). See also Uniroyal Inc. v. Rudkin-Wiley Corp., 5 USPQ2d 1434, 1438-1441 (Fed. Cir.

1988). In fact, it is impermissible to use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. In re Fine, 5 USPQ2d at 1600.

It is respectfully submitted that in making the present rejection under 35 U.S.C. § 103, the Examiner has employed impermissible hindsight in using the Applicant's disclosure and claims to conduct a search of the prior art to locate a reference directed to first and second power transistor stages with first and second collector supply voltages, respectively, and first and second stage bias circuits with third supply and fourth supply voltages (that is, the Yamamoto patent). The Examiner recognized, however, that Yamamoto did not include at least the third and fourth supply voltages. Consequently, the Examiner conducted an additional search to locate a reference that appeared to teach third and fourth supply voltages (that is, the Kuriyama patent). Once Kuriyama was identified, the Examiner concluded that it would have been obvious to one of ordinary skill in the art to modify Yamamoto to include third and fourth supply voltages on the basis on Kuriyama. Given the fundamental differences between the present invention and Yamamoto and/or Kuriyama, however, Applicant respectfully asserts it is not proper to cite Kuriyama simply because Kuriyama allegedly discloses the elements of the claimed invention which the base reference Yamamoto lacks.

Yamamoto uses a feedback system in the biasing circuits. Kuriyama uses a diode bias. Neither reference provides a motivation or a suggestion to combine these references, which are directed to two different biasing circuits.

As understood, the system of Yamamoto is directed to preventing local heating of a transistor array working as a large transistor as typically used in RF power amplifiers. Local

heating or current runaway may occur in a bipolar transistor array due to uneven distribution of bias current or temperature distribution. See, for example, paragraphs 0028-0032 and 0046-0049. The system of Yamamoto relates to employing multiple bias circuitry separately addressing rows and columns of a transistor array with feedback that compensates the amount of bias current addressed to the transistors. See, for example, paragraphs 0058-0051. A power amplifier 1 includes bipolar transistors Q1 and Q2 which have collectors which are biased by voltages VC1 and VC2, respectively. Paragraph 0086. Bias circuits 4 and 5 provided bias current to the respective transistors Q1 and Q2 through the respective base bias resistors Rb1 and Rb2. Paragraph 0084. As shown in Figure 1 of Yamamoto, bias circuit 4 includes transistors Trb11 and Trb12 with the collector of Trb11 biased by the voltage VCC. Similarly, the bias circuit 5 includes transistors Trb21 and Trb22 with the collector of transistor Trb21 biased by the voltage supply VCC. It is asserted in the Office Action that the transistors Trb12 and Trb22 are the second and fourth bias transistors, respectively, recited in claim 1. Further, it is noted in the Office Action that "Yamamoto fails to disclose 'collectors of the second and fourth bias transistors being biased by a third supply voltage.'"

The bias circuits 4 and 5 of Yamamoto are both biased by voltages Vcc and Vpc. The voltage Vpc is applied to the bases of transistors Trb11 and Trb12 and is adjusted such that the bias current to each row and column of the transistor array is uniformly distributed. The voltages of the bias circuit recited in claim 1 are coupled to collectors of the transistors. Thus, the Vpc is not a voltage recited in claim 1. As noted by the Examiner, Yamamoto does not disclose the third supply voltage recited in claim 1.

REPLY UNDER 37 CFR 1.116
-EXPEDITED PROCEDURE-
EXAMINING GROUP 2817

Kuriyama is cited for providing the third supply voltage for biasing the second and fourth bias transistors recited in claim 1. As understood Kuriyama at best merely discloses a high output amplifier that uses a diode-based bias circuit for thermal stability. The bias circuit provides a bias current Ib to the base of the RF transistor RF1. Figure 1. As shown in Figure 2, the bias circuit includes a diode-connected transistor Q1 coupled to the emitter of the transistor Q2. The collector of the transistor Q2 is biased by the supply voltage VCC. A voltage VCONT is a control voltage applied through resistors R1 and R2 to the bases of the respective transistors Q1 and Q2. As shown in Figures 1a and 1b of Kuriyama, a diode is used for DC biasing the RF transistor. The diode-based bias provides thermal stability but has a disadvantage of shortcoming in the linearity performance of the RF circuitry. The bias circuit of Kuriyama compensates the bias current through two paths as shown in Figures 1a and 1b. By supplying a supply voltage VCC of 3.4 volts and a control voltage VCNOT ranging from 2.2 to 3.4 volts, the bias circuit of Kuriyama tries to compensate the bias current Ib. It should be noted that the collector of the RF transistor RF1 is shown in Figure 1 as being biased by a voltage Vc, but this is in error. As noted in Kuriyama on column 4, lines 27-29, a voltage VCC is applied through the inductor L1 to the collector of the transistor RF1. Thus the bias circuit and the power stage of Kuriyama use only two voltages, namely VCONT and VCC. Even if the combination of Yamamoto and Kuriyama were proper, which applicant does not concede, the bias circuit of Kuriyama if applied to the power stage of Yamamoto would not provide the third and fourth supply voltages recited in claim 1. Instead the combination would use the same supply voltage for the collector of the RF transistor and one of the transistors of the bias circuit, which is not the third and fourth supply voltages recited in claim 1.

In support of the combination, the Examiner contends that a person in the art would be motivated to combine the cited references because "The ordinary artisan would have been motivated to modify the circuit of Yamamoto in the manner set forth above for at least the purpose of obtaining high gain and efficiency for the power amplifier." In order to support a rejection under 35 U.S.C. § 103, however, the Examiner must provide "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." In re Fine. The Examiner has not cited an objective prior art reference which provides an incentive, motivation, or suggestion for making the suggested combination. Also, the Examiner has not established by objective evidence that knowledge generally available to one of ordinary skill in the art would lead one to make the suggested combination. It is not sufficient to say the ordinary artisan would be motivated to combine two references to obtain efficiency. Rather under §103, the ordinary artisan must be motivated at the time of the invention to combine the references in the same way as the claims in the patent application. No such motivation is proposed in the Office Action nor can one be found in Yamamoto or Kuriyama. Thus, Applicant respectfully asserts that the suggested combination of Yamamoto and Kuriyama is improper.

For all of the above reasons, Applicant respectfully asserts that claim 1 is patentable over Yamamoto and/or Kuriyama, and that the combination is improper in any case, and therefore respectfully request that the Examiner reconsider and withdraw the rejection. Claim 2 depends from claim 1, and independent claim 6 is generally similar to claim 1. Thus, Applicant respectfully asserts that claims 2 and 6 are also patentable over Yamamoto and/or Kuriyama, and

that the combination is improper in any case, and therefore respectfully request that the Examiner reconsider and withdraw the rejection.

In addition to the above reasons, neither Yamamoto nor Kuriyama, individually or in combination, disclose or even suggest the power amplifier of claim 6. It is asserted in the Office Action that transistors Trb 12 and Trb 11 of Yamamoto are the third and fourth transistors recited in claim 6. Page 4, lines 6-8. Later in the Office Action it is asserted that Kuriyama discloses a resistor coupled between a reference voltage node and a second terminal coupled to the collector of the third transistor Q1 and the base of the fourth transistor Q2. Page 5, lines 15-19. It is unclear whether the transistor Trb12 or the transistor Q1 is being asserted as the third transistor recited in claim 6. Similar uncertainty applies for the linking of the references to the fourth, fifth and sixth transistors recited in claim 6. Claim 6 recites "a first resistor ... including a second terminal coupled to the collector of the third transistor and the base of the fourth transistor". Thus, in the power amplifier recited in claim 6, the collector of the third transistor and the base of the fourth transistor are coupled together. Claim 6 recites "a third inductor including a first terminal coupled to the base of the third transistor and the emitter of the fourth transistor." Thus, the base of the third transistor is coupled to the emitter of the fourth transistor. In contrast the transistors Trb11 and Trb 12 of Yamamoto do not include the base of the transistor Trb 11 being coupled to the emitter of transistor Trb12. Thus, the transistors Trb 11 and Trb 12 cannot be the first and fourth transistors recited in Claim 6. The base of the transistor Q2 of Kuriyama is coupled to the base and collector of the diode connected transistor Q1. The transistors Q1 and Q2 of Kuriyama cannot be the first and fourth transistors recited in Claim 6.

REPLY UNDER 37 CFR 1.116
-EXPEDITED PROCEDURE-
EXAMINING GROUP 2817

The Examiner has rejected claim 5 under the obviousness provisions of 35 U.S.C. §103 as allegedly being unpatentable over Yamamoto in view of Kuriyama and U.S. Patent No. 6,456,163 ("Luo")

Applicant's arguments regarding claims 1, which is the base claim of claim 5, are incorporated herein. Further, Applicant argues that the combination of Luo with Yamamoto and Kuriyama is improper for similar reasons. It is asserted in the Office Action that "the ordinary artisan would have been motivated to modify the circuit of Yamamoto for at least the purpose of adding stability to the system." However there is no teaching or suggestion in either Yamamoto or Luo for combining the bias circuit 3 of Luo to replace the bias circuit 4 and 5 of Yamamoto. The bias circuit 3 and the collector of the power transistor 2 of Luo are biased by the same supply voltage VCC. There is no suggestion in Luo of using different voltages for the bias circuit and the power stage. Combining Luo with Yamamoto or Kuriyama would result in the bias stage and the power stages both being coupled to the same voltage. In contrast, claim 1, which is the base claim of claim 5, uses different voltages for the bias stages and the power stages. Lacking at least this claim feature, neither Yamamoto, Kuriyama, nor Luo, either individually or in combination, can render claim 5 unpatentable. Therefore, it is respectfully submitted that claim 5 is patentable with the references of record. Withdrawal of the rejection is respectfully requested.

The Examiner has rejected claim 7 under the obviousness provisions of 35 U.S.C. §103 as allegedly being unpatentable over Kuriyama in view of U.S. Patent No. 6,052,032 ("Jarvinen").

Claim 7 has been amended merely to correct an informality in response to an objection as noted above.

REPLY UNDER 37 CFR 1.116
-EXPEDITED PROCEDURE-
EXAMINING GROUP 2817

The Examiner cited Figure 3 of Kuriyama as disclosing a power amplifier. Applicant notes that Figure 3 of Kuriyama is a graph. A bias circuit as shown in Figure 1 of Kuriyama includes a diode-connected transistor Q1, or as shown in Figure 1a, a transistor Q1 with a base coupled to its collector through a resistor RR. Claim 7 does not recite a transistor having a base coupled to its collector, either directly or through a resistor. Specially claim 7 recites a "second inductor including a first terminal coupled to the second terminal of the second resistor and including a second terminal coupled to the base of the second transistor and the emitter of the third transistor" and "a third resistor including a first terminal coupled to a reference voltage node and including a second terminal coupled to the collector of the second transistor and the base of the third transistor." It is asserted in the Office Action that the inductor L2 of Kuriyama is the second inductor recited in claim 7. However, the inductor L2 of Kuriyama is coupled to the base and collector of diode connected transistor Q1 and the emitter of transistor Q2, which differs from the second inductor recited in claim 7. It is further asserted in the Office Action that resistor R1 of Kuriyama is the third resistor cited in claim 7. The resistor R1 of Kuriyama is coupled between a voltage VCONT and the common node formed of the base and collector of the diode connector transistor Q1 and the emitter of the transistor Q2. The third resistor of claim 7 is not coupled to the collector of the third transistor. Jarvinen has been cited for disclosing the first resistor, second capacitor, and second resistor recited in claim 7. It is asserted in the Office Action that the resistor Rb/m of Jarvinen is the second resistor recited in claim 7. The resistor Rb/m is coupled between the bias circuit and the base of the RF transistor Q1. The input capacitor is coupled between the RF input (RF-IN) and the base of the transistor Q1. In contrast the second resistor of claim 7 includes the first terminal coupled to the base of the first transistor

and includes a second terminal that is coupled to the second terminal of the second capacitor. This is different than the resistor Rb/m of Jarvinen. There is no suggestion or motivation to modify the circuit of Kuriyama to include the resister Rb/m of Jarvinen for coupling between the inductor L2 and the base of the RF transistor RF1 of Kuriyama, and changing the location of the inductor L2 of Kuriyama to the input side of the capacitor of Jarvinen.

The amplifier of Kuriyama is directed to affecting Class AB biasing of the RF transistor RF1. Column 4, line 32-35. The bias circuit of Kuriyama provides temperature compensation for diode biasing by the transistor Q1. In contrast, the bias circuit of Jarvinen uses a differential amplifier formed of the transistors Qd1 and Qd2 with temperature compensation from the transistor QC. '032 patent, column 3, line 54-column 4, line 9. Because the bias circuits of Kuriyama and Jarvinen are directed to two different types of bias circuits, namely a diode bias circuit and a differential amplifier bias circuit, there is no suggestion or teaching in either reference for combining specific elements of Jarvinen (namely the capacitor, the resistor Rb/m and the resistor Re/m), with the high output amplifier of Kuriyama. Lacking the disclosure or even suggestion of at least this claim feature, neither Kuriyama nor Jarvinen, either individually or in combination, render claim 7 unpatentable. Therefore, it is respectfully submitted that claim 7 is patentable over the references of record. Withdrawal of the rejection is respectfully requested.

Claims 3-4 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Because base claim 1 is deemed allowable for the foregoing

reasons, it is respectfully submitted that claims 3-4 are allowable without being rewritten. Withdrawal of the objection to and allowance of claims 3-4 are requested.

New claim

Claim 8 has been added and is submitted to be patentable for the same reasons submitted above for base claim 1. No new matter has been added.

Conclusion

Applicant believes that all of the stated grounds of objection and rejection set forth by the Examiner in the Office Action have been properly accommodated or addressed. Applicant, therefore, respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and withdraw them. The Examiner is invited to telephone the undersigned representative if it is felt that an interview might be useful for any reason.

Respectfully submitted
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